AMENDMENTS TO THE CLAIMS:

Please amend claims 1, 2 4, and 53, 54 and add newly written claim 55 as follows:

1. *(Currently Amended)* A photodetector circuit comprising:

a photodiode detector, said photodetector having a PN structure with p-type and n-type active regions;

a readout circuit, said readout circuit at least partly incorporated in a CMOS component and having a guard ring delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown; and

a deposited epitaxial layer supported by said CMOS component, said epitaxial layer providing only one of said active regions, said ~~photodiode detector, in response to said only one active region, having~~readout circuit and said epitaxial layer adapted to provide a gradual knee in a current-voltage characteristic.

2. *(Currently Amended)* A photodetector circuit according to Claim 1 wherein the CMOS component comprises a substrate supporting and insulated from at least a portion of said CMOS readout circuit, the photodiode detector is operable in current multiplication mode and the epitaxial layer is deposited upon the substrate.

3. *(Previously Presented)* A photodetector circuit according to Claim 39, wherein the epitaxial layer provides a high field region.

4. *(Currently Amended)* A photodetector circuit according to Claim 2 wherein the photodiode detector is an avalanche photodiode and said photodiode active regions

comprise ~~a first~~one active region incorporated in the substrate, and the epitaxial layer is a layer deposited upon the ~~first~~one active region and provides ~~a second~~the other active region of the photodiode.

5. Cancelled

6. Cancelled

7. *(Previously Presented)* A photodetector circuit according to Claim 1 wherein said readout circuit is arranged to provide said photodiode detector with a logarithmic response to incident radiation.

8. *(Previously Presented)* A photodetector circuit according to Claim 1, wherein said readout circuit incorporates parasitic photodiodes, arranged in series with said readout circuit, for contributing to circuit output in response to incident radiation.

9. *(Previously Presented)* A photodetector circuit according to Claim 1, wherein said readout circuit includes an amplifier arranged in a feedback loop for providing feedback to stabilise photodiode detector bias voltage.

10. *(Previously Presented)* A photodetector circuit according to Claim 9, wherein the amplifier is arranged to amplify an output signal from the photodiode detector and to provide feedback to bias a load transistor in series with the photodiode detector.

11. *(Previously Amended)* A photodetector circuit according to Claim 10, wherein

the amplifier is a push-pull amplifier.

12. *(Previously Presented)* A photodetector circuit according to Claim 10, wherein said readout circuit includes a cascode transistor arranged to reduce Miller Effect capacitance in the amplifier.

13. *through 37 Cancelled*

38. *(Previously Presented)* A photodetector circuit comprising:

a photodiode detector, said photodetector having a PIN structure, said structure having first, second and third active regions, one active region p-type, one active region substantially undoped and one active region n-type;

a readout circuit, said readout circuit at least partly incorporated in a CMOS component and having a guard ring delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown; and

a deposited epitaxial layer supported by said CMOS component, said epitaxial layer providing only one of said active regions, said photodiode detector, in response to said only one active region, having a gradual knee in a current-voltage characteristic.

39. *(Previously Presented)* A photodetector circuit according to Claim 38 wherein the readout circuitry incorporates CMOS circuitry, the CMOS component comprises a substrate supporting and insulated from said CMOS circuitry, the photodiode detector is operable in current multiplication mode and the epitaxial layer is deposited upon the substrate.

40. *Cancelled*

41. *(Previously Presented)* A photodetector circuit according to Claim 39, wherein the epitaxial layer comprises a first epitaxial layer supporting a second epitaxial layer, said first epitaxial layer providing said second active region and said second epitaxial layer, on said first epitaxial layer, comprising said third active region of the photodiode,.

42. *(Previously Presented)* A photodetector circuit according to Claim 41, wherein the third active region is electrically connected to the guard ring and has like potential therewith during circuit operation.

43. *(Previously Presented)* A photodetector circuit according to Claim 38, wherein said readout circuit includes at least one circuit element arranged to provide said photodiode detector with a logarithmic response to incident radiation.

44. *(Previously Presented)* A photodetector circuit according to Claim 38, wherein said readout circuit incorporates parasitic photodiodes arranged in series with said readout circuit, for contributing to circuit output in response to incident radiation.

45. *(Previously Presented)* A photodetector circuit according to Claim 38, wherein said readout circuit includes an amplifier arranged in a feedback loop for providing feedback to stabilise photodiode detector bias voltage.

46. *(Previously Presented)* A photodetector circuit according to Claim 45,

wherein the amplifier is arranged to amplify an output signal from the photodiode detector and to provide feedback to bias a load transistor in series with the photodiode detector.

47. *(Previously Presented)* A photodetector circuit according to Claim 46, wherein the amplifier is a push-pull amplifier.

48. *(Previously Presented)* A photodetector circuit according to Claim 46, wherein said readout circuit includes a cascode transistor arranged to reduce Miller Effect capacitance in the amplifier.

49. *(Previously Presented)* A photodetector circuit according to Claim 38, wherein the CMOS component is a substrate supporting and insulated from CMOS circuitry, the photodiode detector comprises a region of one conductivity type incorporated in the substrate, and the epitaxial layer comprises a first epitaxial layer supporting a second epitaxial layer, one of said epitaxial layers is substantially undoped and the other of said epitaxial layers is of opposite conductivity type to that of the region incorporated in the substrate, the region in the substrate and the two epitaxial layers comprising a PIN diode.

50. *(Previously Presented)* A photodetector circuit according to Claim 49, wherein the undoped epitaxial layer is one of a SiGe alloy and a quantum well structure of the $Si_{1-x}Ge_x$ material system where the value of the compositional parameter x changes

between successive layers.

51. *(Previously Presented)* An array of photodetector circuits, each photodetector circuit comprising:

a photodiode detector, said photodiode detector having a PN structure with p-type and n-type active regions;

a readout circuit, said readout circuit being at least partly incorporated in a CMOS component and having a guard ring delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown; and

a deposited epitaxial layer supported by the CMOS component, the epitaxial layer providing only one of said active regions of the photodiode detector, the photodiode detector, in response to said only one active region, having a gradual knee in a current-voltage characteristic.

52. *(Previously Presented)* An array of photodetector circuits, each photodetector circuit comprising:

a photodiode detector, said photodiode detector having PIN structure, said structure having three active regions, one active region p-type, one active region substantially undoped and one active region n-type;

a readout circuit, said readout circuit being at least partly incorporated in a CMOS

component and having a guard ring delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown; and

a deposited epitaxial layer supported by the CMOS component and providing only one of said active regions of the photodiode detector, the photodiode detector, in response to said only one active region, having a gradual knee in a current-voltage characteristic.

53. *(Currently Amended)* A method of making a photodetector circuit including a photodiode detector, comprising the steps of:

forming at least part of a readout circuit as a CMOS component, the readout circuit having a guard ring for delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown; and a photodiode detector,

forming a deposited epitaxial layer supported by the CMOS component to produce ~~a~~said photodiode detector having a PN structure with p-type and n-type active regions, the epitaxial layer providing only one of said active regions, the photodiode detector, in response to said only one active region, having a gradual knee in a current-voltage characteristic.

54. *(Currently Amended)* A method of making a photodetector circuit including a photodiode detector comprising the steps of:

forming at least part of a readout circuit as a CMOS component, the readout circuit having a guard ring for delimiting and surrounding the photodiode detector for

enhancing electric field uniformity and inhibiting breakdown; and a photodiode detector,

forming a deposited epitaxial layer supported by the CMOS component to produce ~~a~~said photodiode detector having PIN structure with three active regions, one active region p-type, one active region substantially undoped and one active region n-type, the epitaxial layer providing only one of said active regions, the photodiode detector, in response to said only one active region, having a gradual knee in a current-voltage characteristic.

55. *(New)* An array of photodetector circuits, each photodetector circuit comprising:

a photodiode detector, said photodiode detector having a PIN structure, said structure having three active regions, a first active region which is p-type, a second active region which is substantially undoped and a third active region which is n-type;

a readout circuit, said readout circuit at least partly incorporated in a CMOS component hand having a guard ring delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown, said first active region being incorporated in the CMOS component;

said second active region being a first epitaxial layer deposited upon said first active region and providing and being coextensive in thickness with said second active region;

said third active region being a second epitaxial layer deposited upon said second active region and providing and being coextensive in thickness with said third active region; and

respective conductivity junctions occurring at interfaces between said first epitaxial layer and said first active region and between said first epitaxial layer and said second epitaxial layer, the photodiode detector, in response to said first epitaxial layer and said second epitaxial layer, having a gradual knee in a current-voltage characteristic.